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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,190	09/16/2003	Yervant Zorian	4640P019	3960

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,190	ZORIAN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a **FINAL OFFICE ACTION** in response to Amendment filed 12/11/2006.

Claims 1-30 are presently under examination and still pending in the Application.

The objection to the specification, with respect to the title of the invention as being not descriptive, has been withdrawn in view of a new title.

Rejection of Claims 1-11, 15, 30 under 35 U.S.C. 112, second paragraph, has been withdrawn in view of Applicant's arguments and amendments to the claims.

Response to Arguments

Applicant's arguments, see Amendment filed 12/11/2006, with respect to the rejections of claims under 35 U.S.C. 102(e) as being anticipated by White et al. (US Patent No. 7,007,211) and under 35 U.S.C. 103(a) as being unpatentable over White et al. (US Patent No. 7,007,211) in view of Hayashi et al. (US Patent No. 6,779,144), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Applicant's arguments with respect to claims 1-30 are moot in view of the new grounds of rejection, as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following Claims recite the limitations:

Claim 1, "that memory".

Claim 12, "that memory", "associated with that command".

Claim 16, "that particular memory".

Claim 21, "bounding that memory", "that command".

These limitations render the claims indefinite because of insufficient antecedent basis due to the term "that". Change term "that" to --the--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 and 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Pendurkar (US 20040006729), 10/189870, filed: July 3, 2002.

Regarding independent Claim 1, Pendurkar discloses an apparatus, Fig. 5, comprising:

Two or more memories (memory arrays) 508(1)-(m) each located in a corresponding (testable memory element) 506(1)-506(m), wherein each memory element 506 is a BIST-enabled memory structure that includes an intelligence wrapper (memory BIST controller 510) coupled to a corresponding memory array 508.

A processor (master BIST controller, MBC 504), which decodes the BIST control mode signals and, in response, selectively asserts BIST_EN for the (memory arrays) 508(1)-(m) located in the corresponding memory elements 506(1)-506(m) to initiate testing operations.

A serial bus (516) coupled between the processor (MBC) 504 and each memory 506(1)-506(m), wherein the processor (MBC) 504 load commands (600, 610, 620, Figs. 6a, b and c) via the serial bus 516 by decoding the BIST control mode signals and, in response, selectively asserts BIST_EN for core memory elements 506(1)-506(m) to initiate testing operations. MBC 504 may schedule either concurrent or sequential BIST operations in the corresponding core memory elements 506, (see, Paragraph 38).

The command comprises representations of a "March" element and data (610, 620, Figs. 6b and c). A UDR 303b, referred to as the control mode register, stores a number of algorithm mode bits that indicate which algorithm (e.g., a 6N or 13N March algorithm) the BIST operations performed in MCC 300 utilize, a test mode bit that indicates whether the BIST operation in cores 308 are performed concurrently or sequentially, and other control information, (see, Paragraph 33).

Regarding Claims 2-8, Pendurkar discloses a first intelligence wrapper (memory BIST controller) 510 (1) executes a set of test vectors corresponding to memory array 508 (1) as described in Paragraph [0045]. "MBC 504 for each selected core 308 decodes the instruction received from chip MBC 304 and provides an asserted BIST_EN to the memory BIST controllers 510 in corresponding core memory elements 506. Memory BIST controllers 510 perform a well-known memory BIST operation on corresponding memory arrays 508 in response to BIST_EN received from core MBC 504. After testing, each memory BIST controller 510 returns a done signal and a pass/fail signal to chip MBC 304 via core MBC 504 and core TAP controller 502. The done signal indicates whether the test operation is complete, and the pass/fail signal indicates whether a fault is detected in the corresponding memory array.

Regarding Claims 9-11, Pendurkar discloses each memory BIST controller 510 includes an address generator and a test register to store test patterns that may be applied to memory array 508 during BIST operations. The test patterns read out of memory arrays 508 are compared with an expected result or signature in a well-known manner, for example, using comparators and multiple-input shift registers (MISR) provided within memory BIST controllers 510. If the output test patterns match the expected signature, the pass/fail signal is asserted to indicate the pass condition. Otherwise, the pass/fail signal is de-asserted to indicate the fail condition.

Regarding independent Claims 25, 28, Pendurkar discloses a method and apparatus that allow processor cores with standard test architectures to be replicated on

a multi-core chip (MCC) without modification that allows for chip level access to internal BIST circuitry in the processor cores, see, Paragraph [0008], Figs. 5 and 7, comprising:

Compressing information using (master BIST controller) MBC 504, which sends compressed information in the form of serial data for self testing of (memory arrays) 508(1)-(m) in (memory elements) 506(1)-506(m) embedded in a single integrated circuit (IC) known as a multi-core chip (MCC) 300, Fig. 3 and also shown as a processor core 500, Fig. 5.

Communicating the compressed information via a serial bus (516) to logic (memory BIST controller 510) coupled to the memory array 508 in the (memory element) 506, Fig. 5.

Regarding Claims 26, 27, 29, 30, Pendurkar discloses expanding the compressed information to a parallel-decompressed information using (memory BIST controller) 510 (1) to perform the self-test on one or more addresses in the memory. Memory BIST controller 510 (1) executes a set of test vectors corresponding to memory array 508 (1) as described in Paragraph [0045]. "MBC 504 for each selected core 308 decodes the instruction received from chip MBC 304 and provides an asserted BIST_EN to the memory BIST controllers 510 in corresponding core memory elements 506. Memory BIST controllers 510 perform a well-known memory BIST operation on corresponding memory arrays 508 in response to BIST_EN received from core MBC 504. After testing, each memory BIST controller 510 returns a done signal and a pass/fail signal to chip MBC 304 via core MBC 504 and core TAP controller 502. The

done signal indicates whether the test operation is complete, and the pass/fail signal indicates whether a fault is detected in the corresponding memory array.

Regarding independent Claims 12, 21, Pendurkar discloses an apparatus and method, Figs. 5 and 7, comprising:

Two or more memories (memory arrays) 508(1)-(m) each located in a corresponding (testable memory element) 506(1)-506(m), wherein each memory element 506 is a BIST-enabled memory structure that includes an intelligence wrapper (memory BIST controller 510) coupled to a corresponding memory array 508.

A processor (master BIST controller, MBC 504), which decodes the BIST control mode signals and, in response, selectively asserts BIST_EN for the (memory arrays) 508(1)-(m) located in the corresponding memory elements 506(1)-506(m) to initiate testing operations.

A serial bus (516) coupled between the processor (MBC) 504 and each memory 506(1)-506(m), wherein the processor (MBC) 504 load commands (600, 610, 620, Figs. 6a, b and c) via the serial bus 516 by decoding the BIST control mode signals and, in response, selectively asserts BIST_EN for core memory elements 506(1)-506(m) to initiate testing operations. MBC 504 may schedule either concurrent or sequential BIST operations in the corresponding core memory elements 506, (see, Paragraph 38).

With respect to the claimed limitation of the processor sending a command to the first intelligence wrapper at a first speed and the control logic executing the operations associated with the command at a second speed asynchronous with the first speed, Pendurkar discloses a processor (master BIST controller, MBC 504), which includes a

clock operating at a first speed (low speed) for sending the command to the intelligence wrapper (memory BIST controller 510) at low a speed. Memory BIST controller 510 includes a clock operating at a second speed (high speed) which executes test vectors for testing the (memory array) 508 at the (high speed) corresponding to the functional sped of the memory array. The two speeds are asynchronous with respect to each other, since each speed is generated by asynchronous clock.

Regarding Claims 13-19, 21-24, Pendurkar discloses a first intelligence wrapper (memory BIST controller) 510 (1) executes a set of test vectors corresponding to memory array 508 (1) as described in Paragraph [0045]. "MBC 504 for each selected core 308 decodes the instruction received from chip MBC 304 and provides an asserted BIST_EN to the memory BIST controllers 510 in corresponding core memory elements 506. Memory BIST controllers 510 perform a well-known memory BIST operation on corresponding memory arrays 508 in response to BIST_EN received from core MBC 504. After testing, each memory BIST controller 510 returns a done signal and a pass/fail signal to chip MBC 304 via core MBC 504 and core TAP controller 502. The done signal indicates whether the test operation is complete, and the pass/fail signal indicates whether a fault is detected in the corresponding memory array.

Regarding Claim 20, Pendurkar discloses command comprises representations of a "March" element and data (610, 620, Figs. 6b and c). A UDR 303b, referred to as the control mode register, stores a number of algorithm mode bits that indicate which algorithm (e.g., a 6N or 13N March algorithm) the BIST operations performed in MCC

300 utilize, a test mode bit that indicates whether the BIST operation in cores 308 are performed concurrently or sequentially, and other control information (Paragraph 33).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

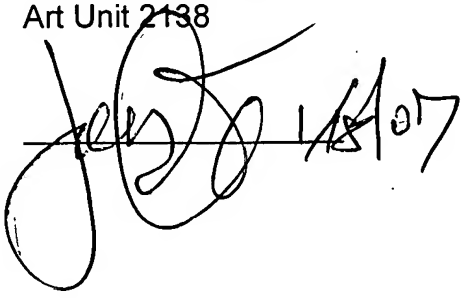
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



Date: 18 January 2007
Office Action: Final Rejection

U.S. Patent and Trademark Office
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov